Les circuits logiques programmables

1) INTRODUCTION

Les circuits logiques programmables ont fait leur apparition au début des années 80.

2) TERMINOLOGIE

Abréviations couramment utilisées:

EPLD: Erasable Programmable Logic Device

FPGA: Field Programmable Gate Array

GAL: Generic Array Logic

LCA: logic Cell Array

MACH: Macro Array Cmos High density

PAL: Programmable Array Logic

PLD: Programmable Logic Device

PGA: Programmable Gate Array

CPLD: Complex Programmable Logic Device

3) Quelques fabricants

Haut niveau d ’intégration:

Altera

Xilinx

Actel

Atmel

...

4) TECHNOLOGIES

Selon les fabricants on trouve des circuits:

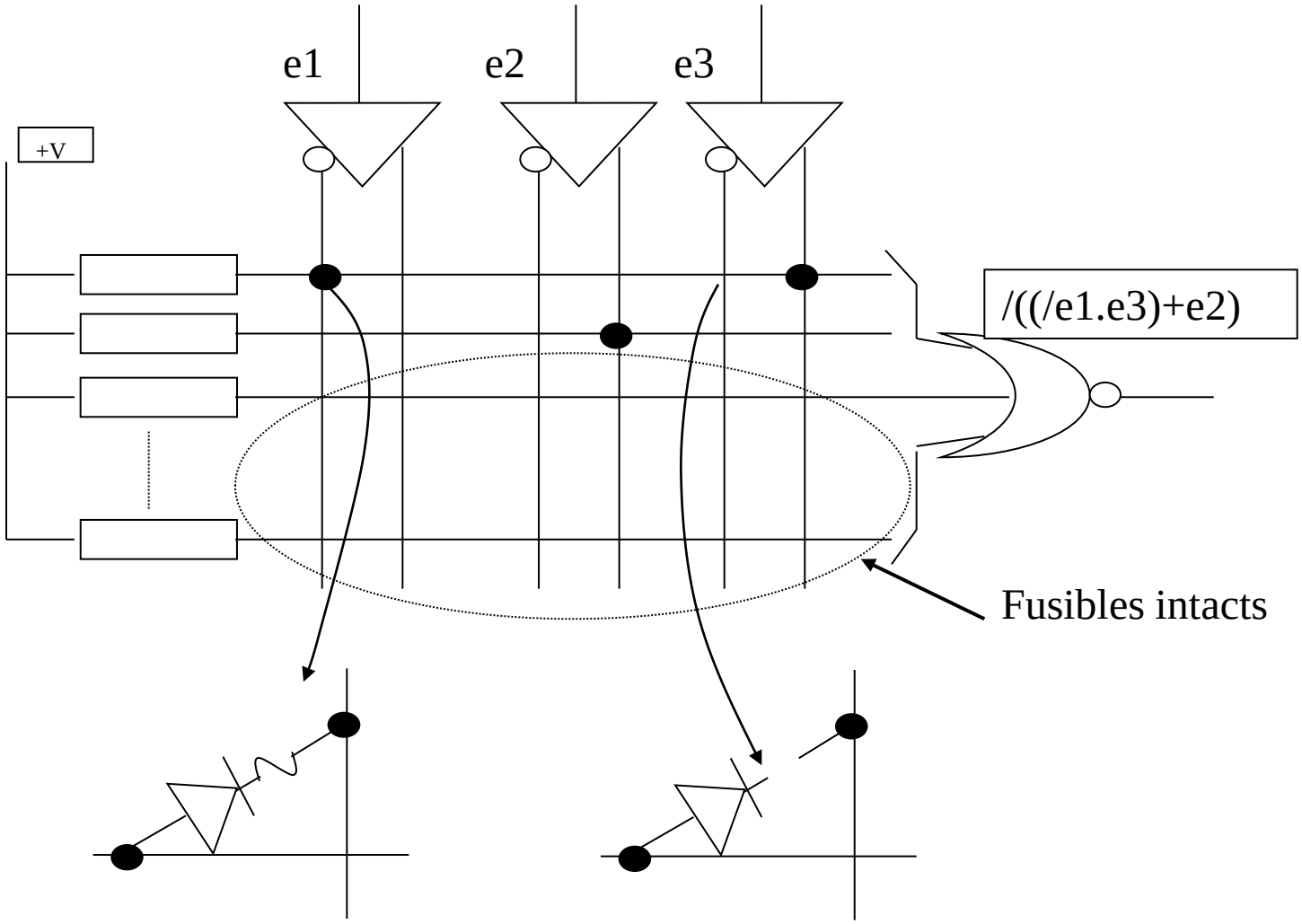
- OTP (One Time Programmable) constitués de matrices à fusibles (ou anti-fusibles). (très peu utilisés aujourd'hui!)

- Effaçables aux U.V. (type EPROM). (quasiment plus utilisés!)

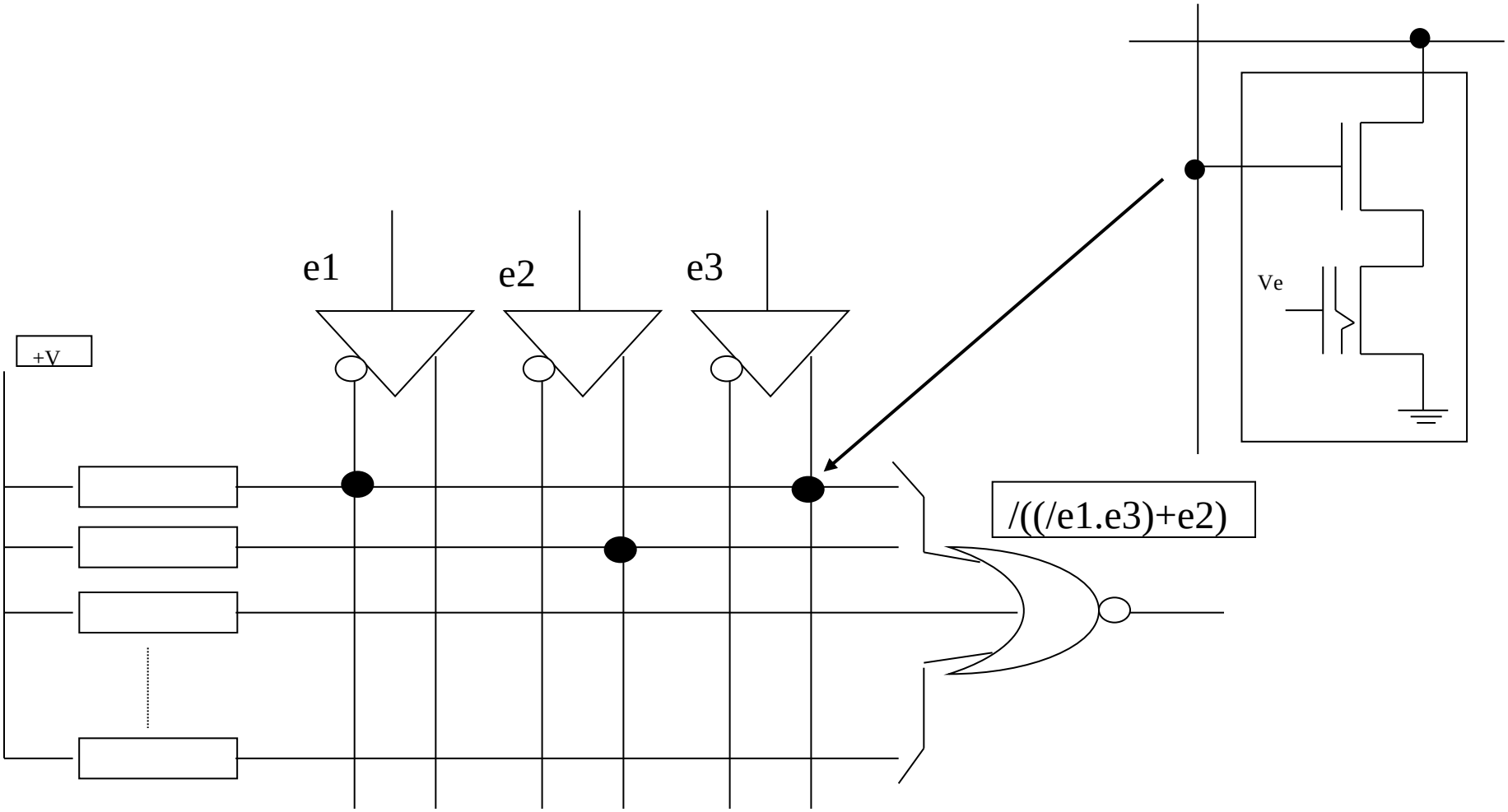
- Effaçables électriquement (EEPROM).

- Programmables par RAMs statiques. (les plus utilisés: faible consommation)

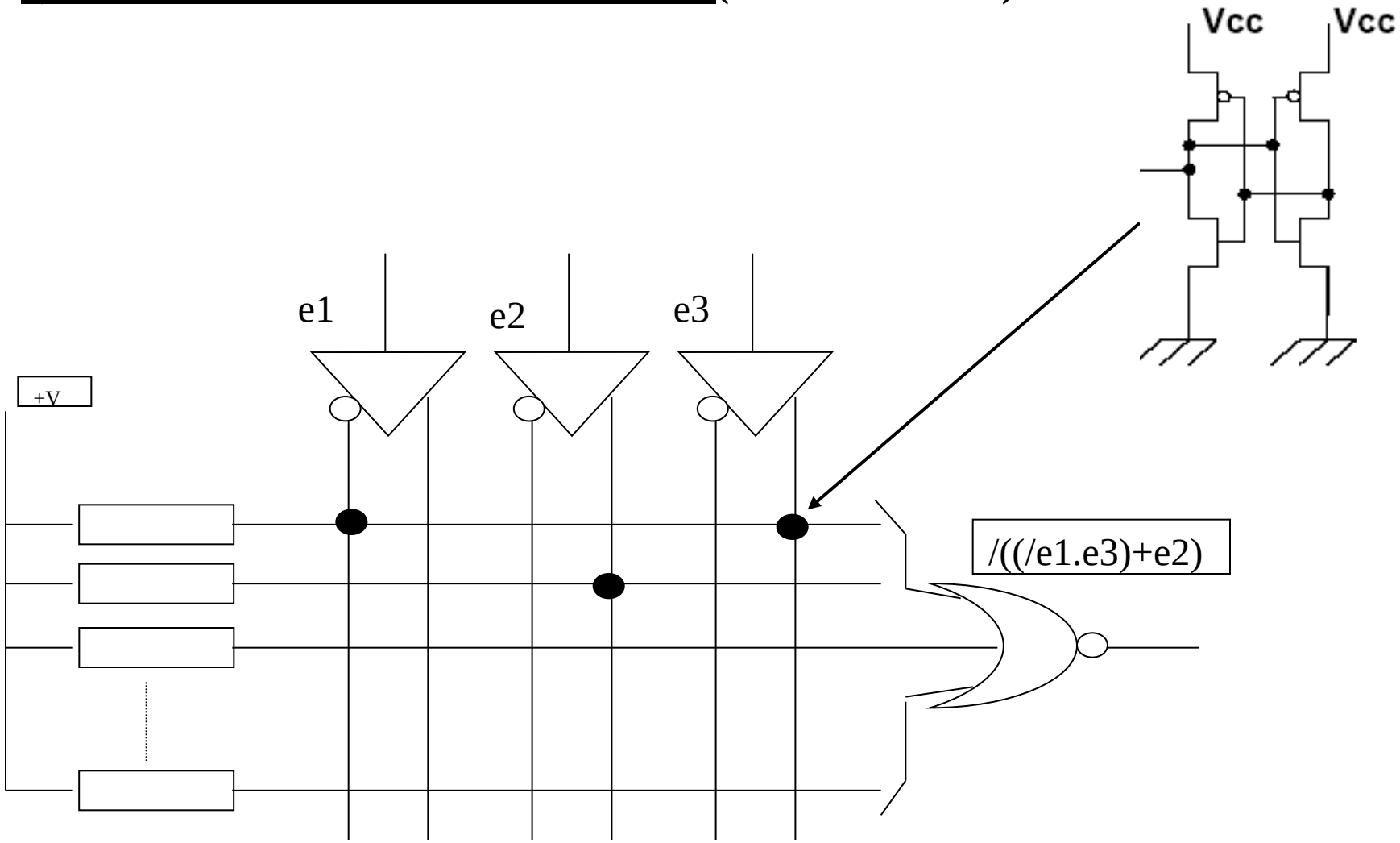
5) PRINCIPE DE PROGRAMMATION (fusibles)



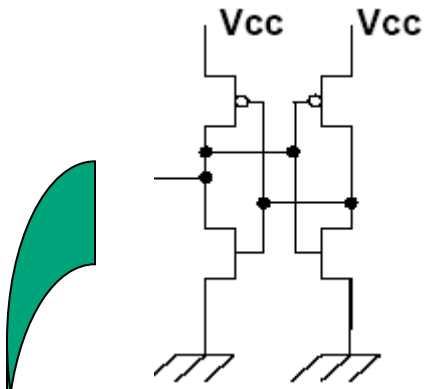
5) PRINCIPE DE PROGRAMMATION (transistors MOS à grille flottante)



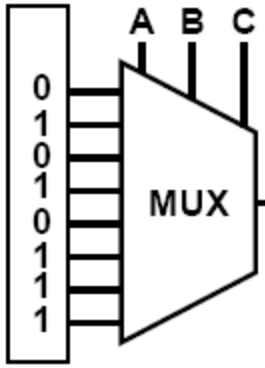
5) PRINCIPE DE PROGRAMMATION (Mémoire SRAM)



5) Evolution principe de programmation (SRAM + multiplexeur ou LUT)



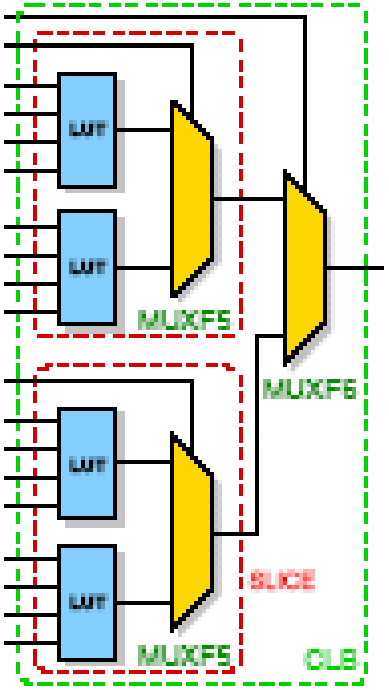
3 entrées logiques



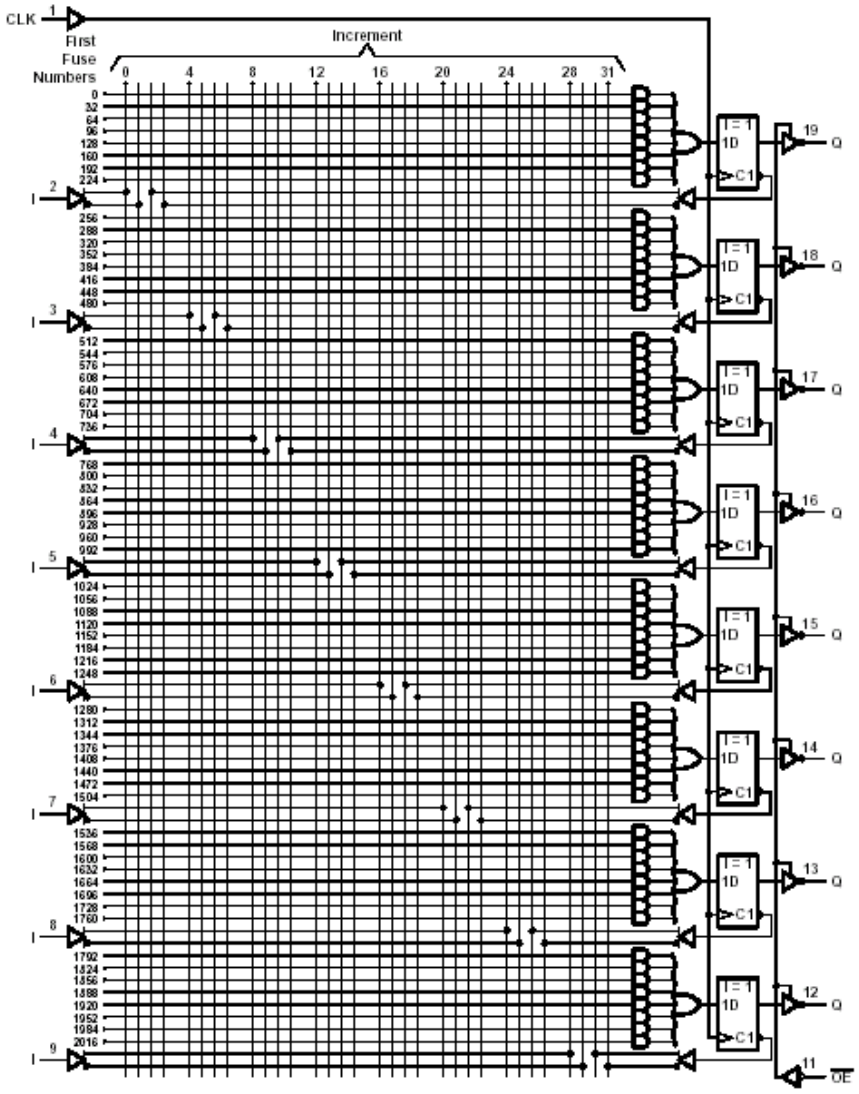
S = f (A,B,C)

8 cellules SRAM

Bloc de LUT 4 entrées

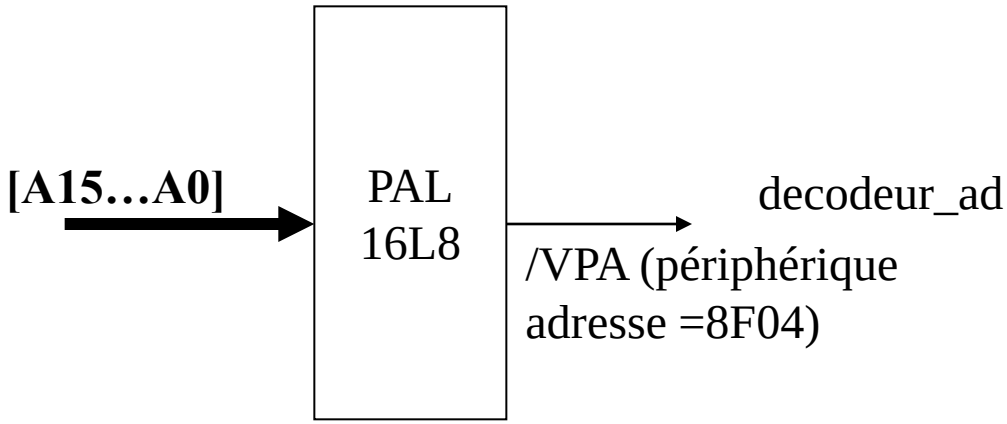


6) Circuits SSI: MMI PAL 16R8 ARCHITECTURE



Les circuits logiques programmables

APPLICATION: Le décodage d 'adresses.



Brochage:

pin 1:A15	pin 11:A6
pin 2:A14	**pin12:/VPA**
pin 3:A13	pin 13:A5
pin 4:A12	pin 14:A4
pin 5:A11	pin 15:A3
pin 6:A10	pin 16:A2
pin 7:A9	pin 17:A1
pin 8:A8	pin 18:A0
pin 9:A7	

Equation:

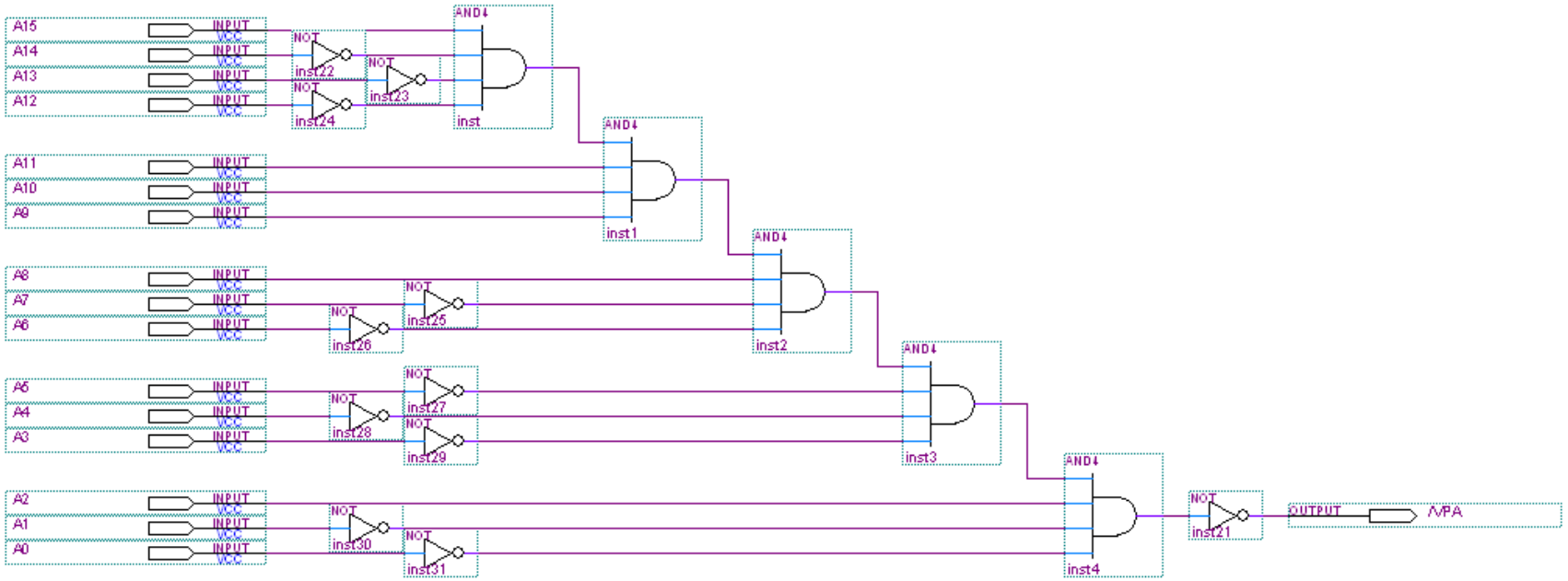
/VPA=A15*/A14*/A13*/A12*A11*A10*A9*A8*/A7*/A6*/A5*/A4*/A3*A2*/A1*/A0

=> Gain de temps de propagation

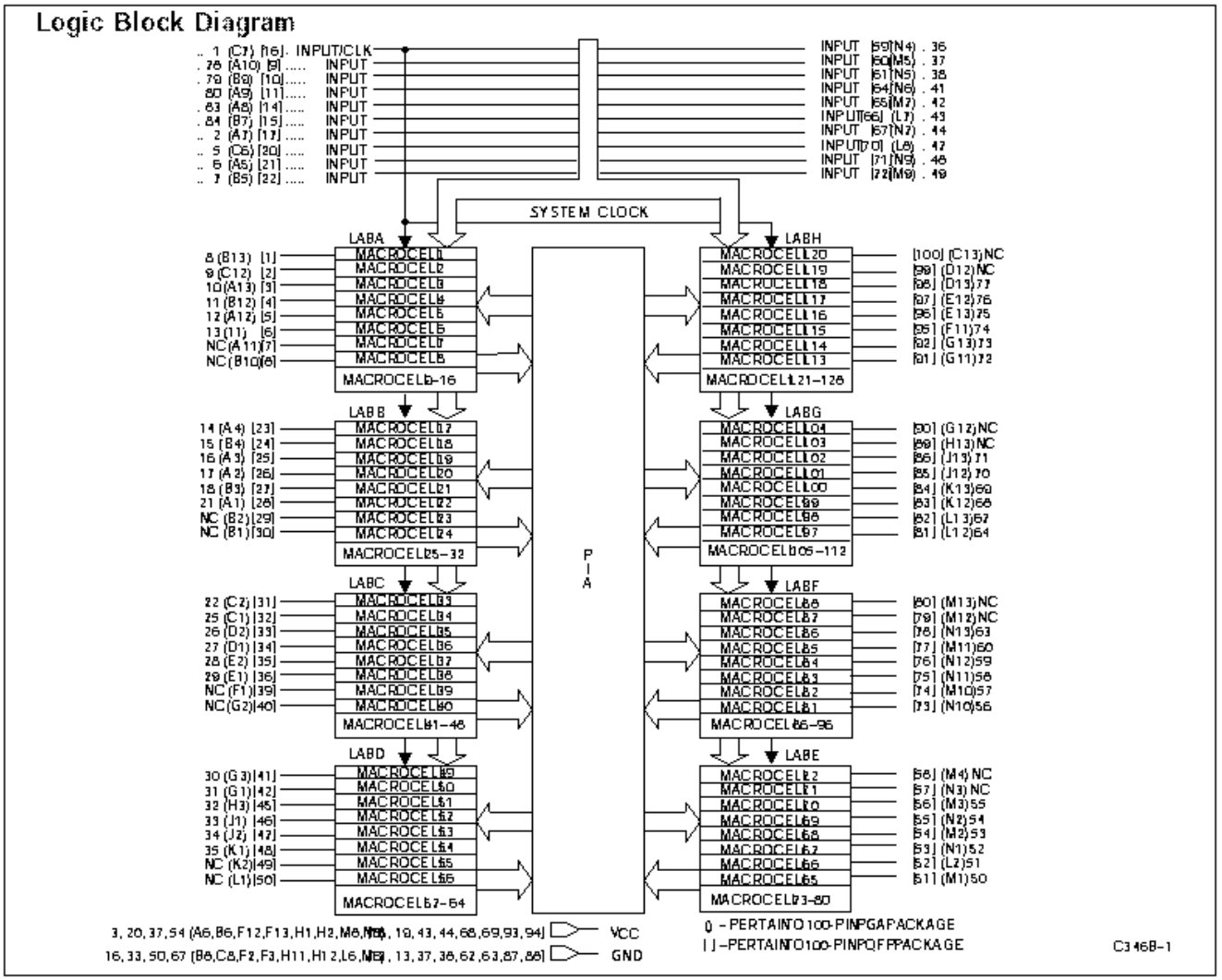
APPLICATION: Le décodage d 'adresses.

Equation:

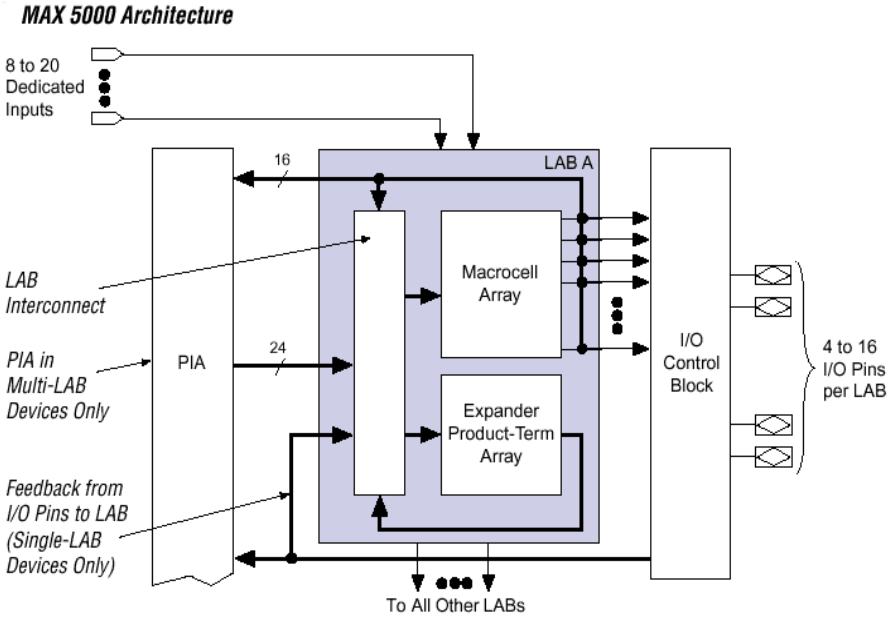
/VPA=A15*/A14*/A13*/A12*A11*A10*A9*A8*/A7*/A6*/A5*/A4*/A3*A2*/A1*/A0

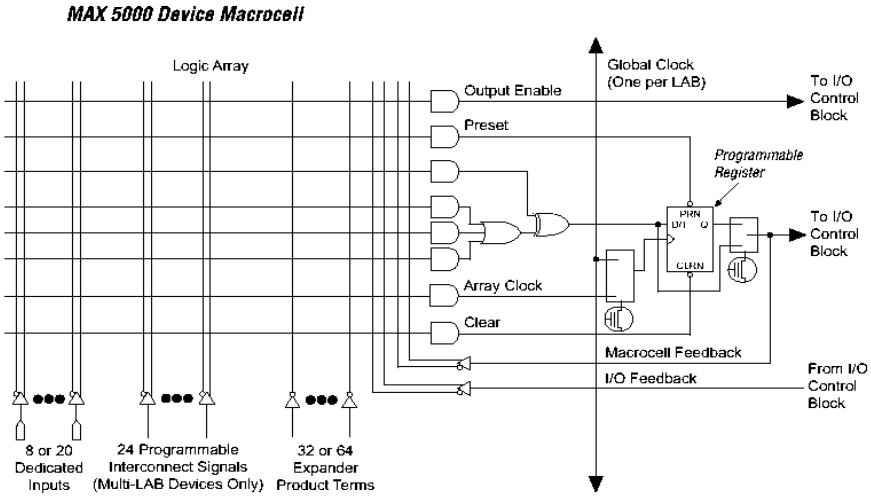


7) Circuits LSI: ALTERA série 5000 ARCHITECTURE

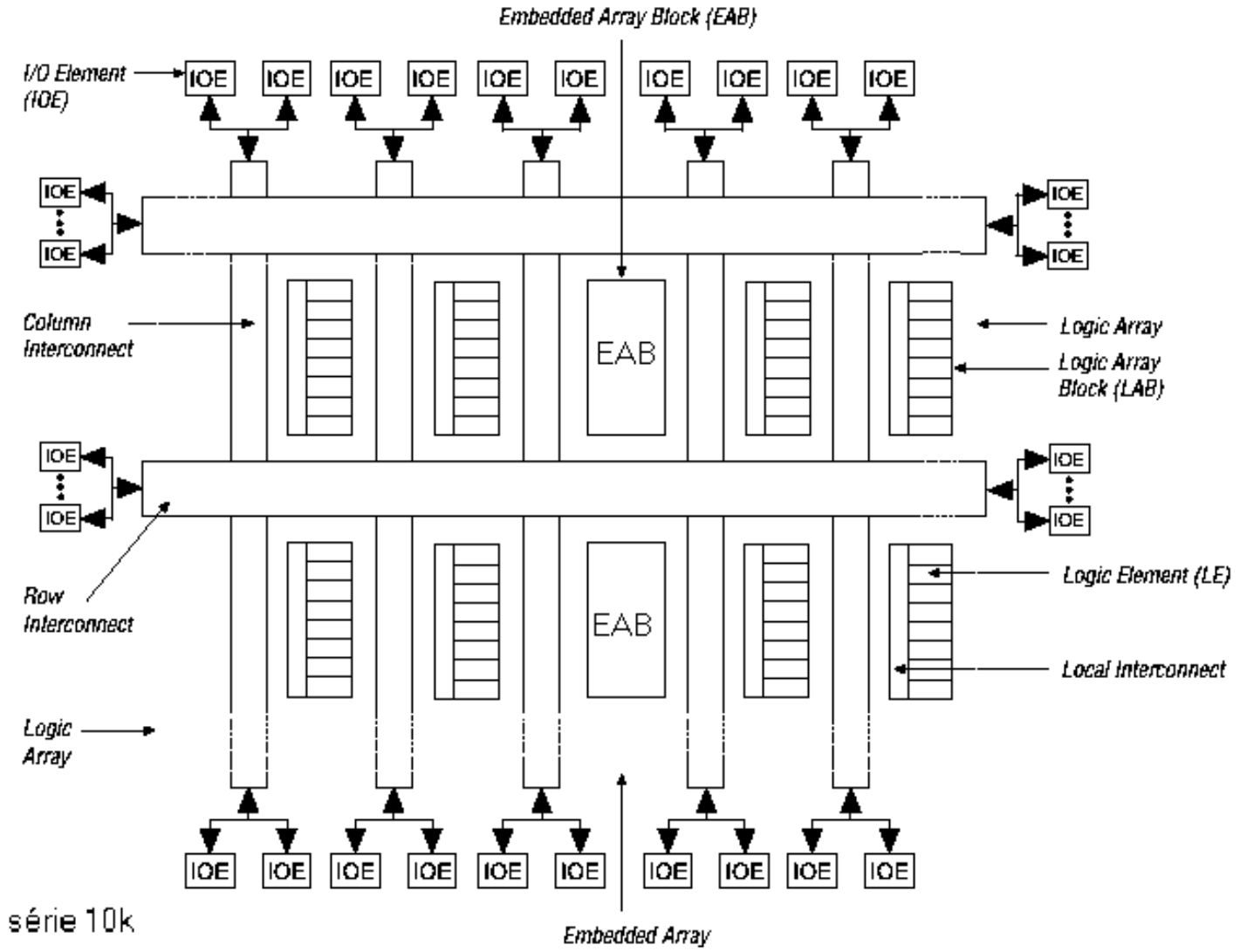


7) Circuits LSI: ALTERA série 5000

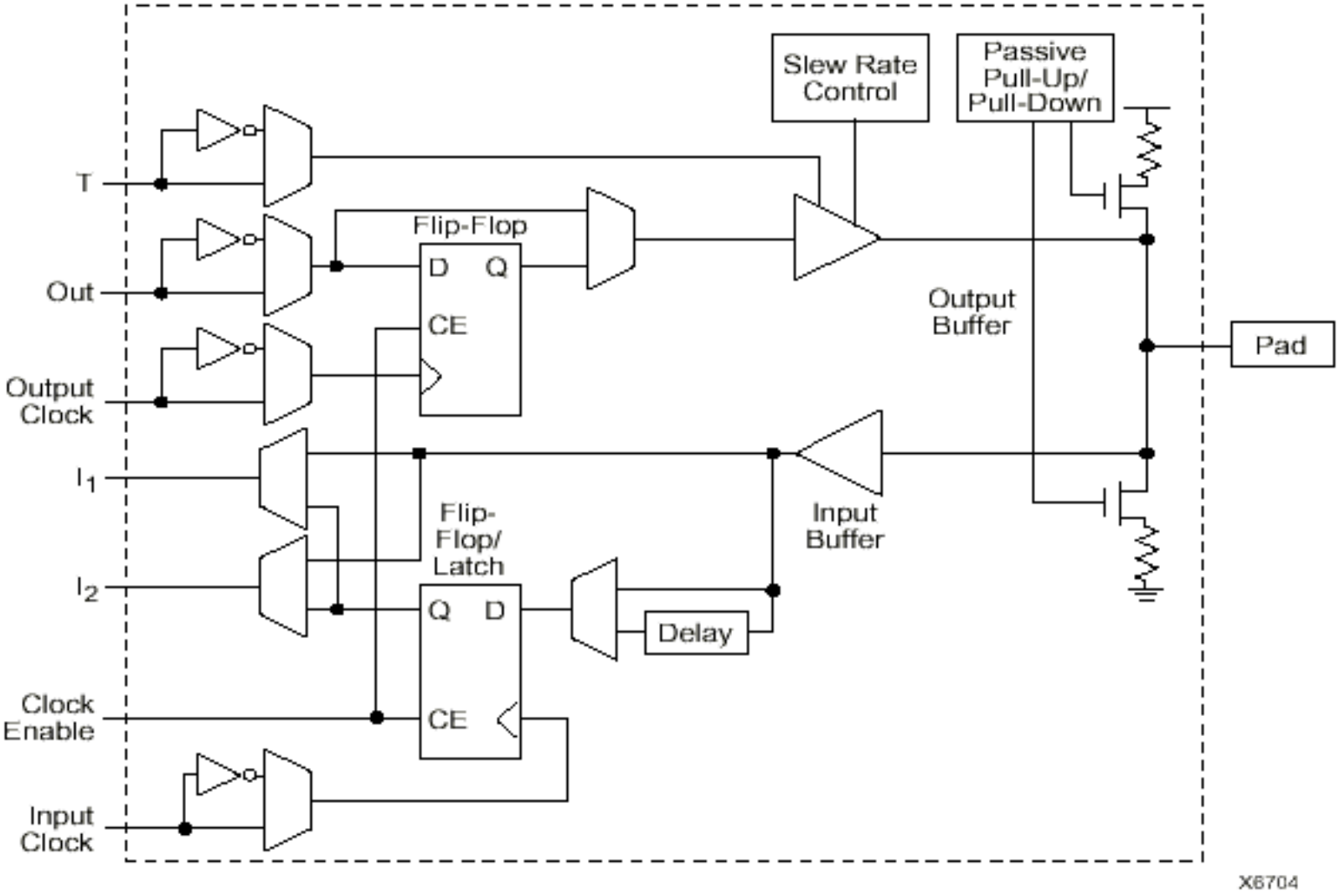




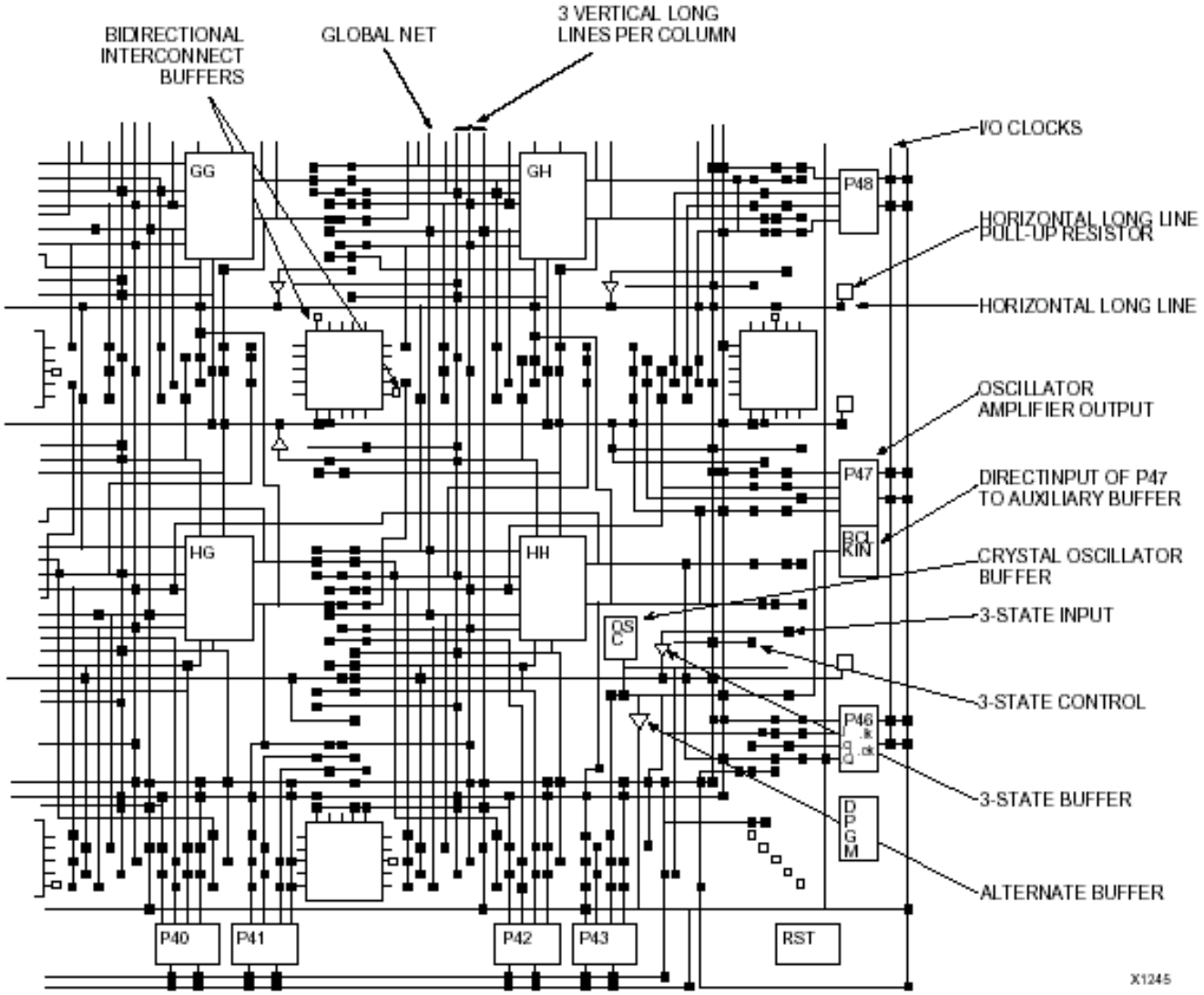
7) Circuits LSI: ALTERA série 10k



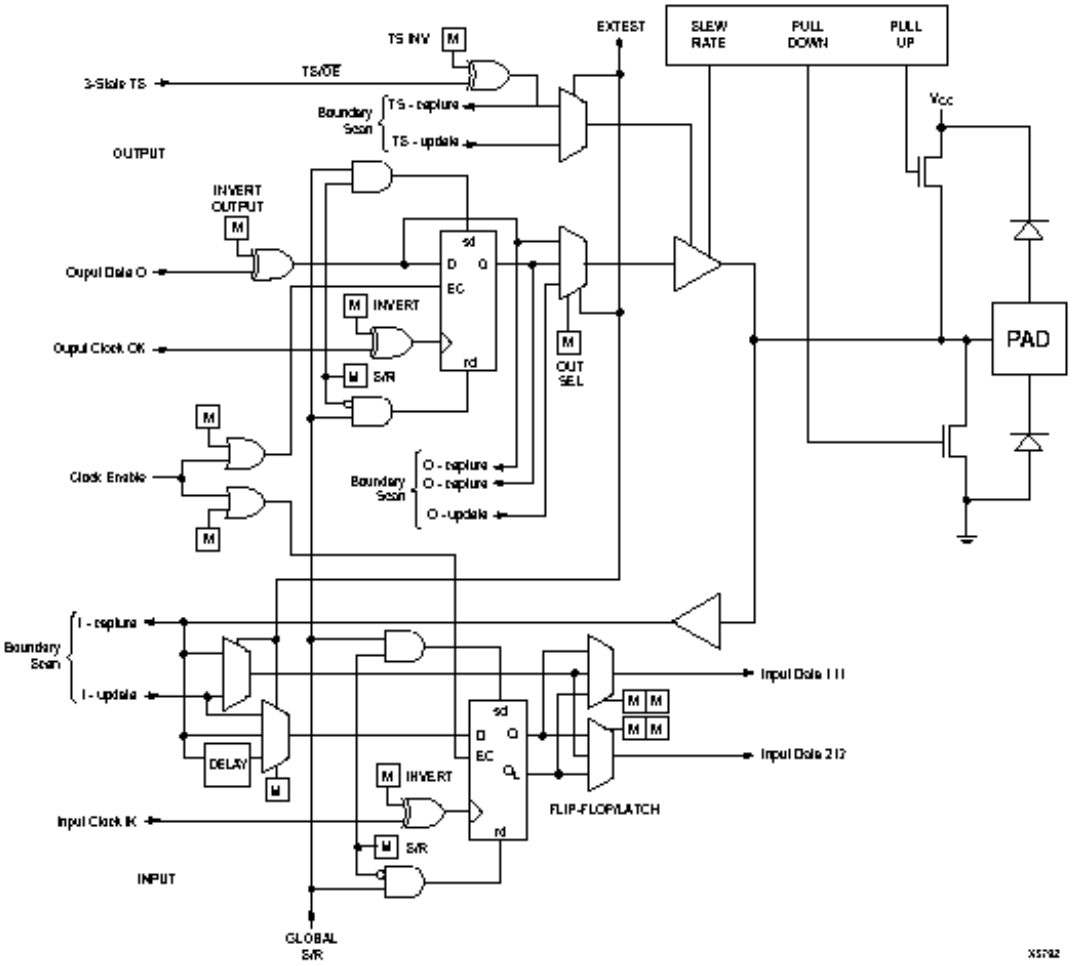
7) Circuits LSI: XILINX famille 3000 : Macro-cellule type



7) Circuits LSI: XILINX famille 3000 Routage des macro-cellules

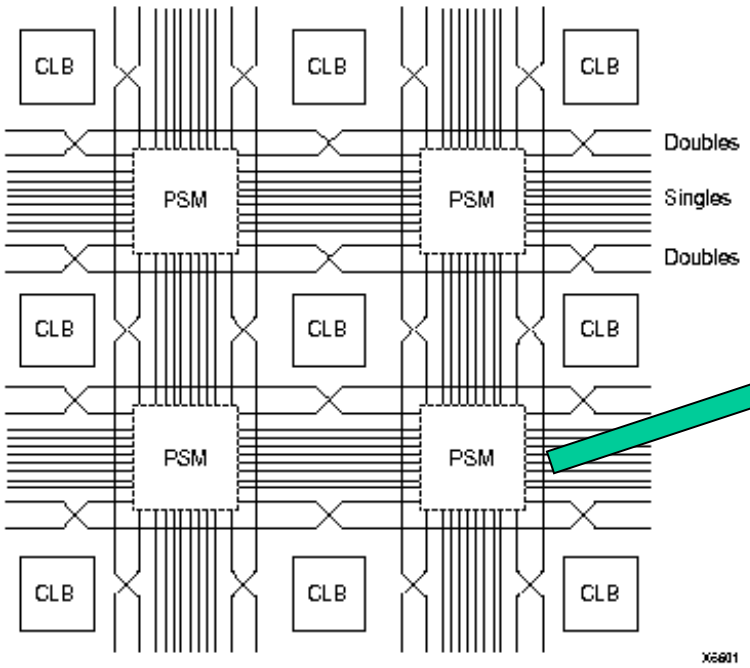


7) Circuits LSI: XILINX famille 4000 Bloc E/S



7) Circuits LSI: XILINX famille 4000

Structure interne



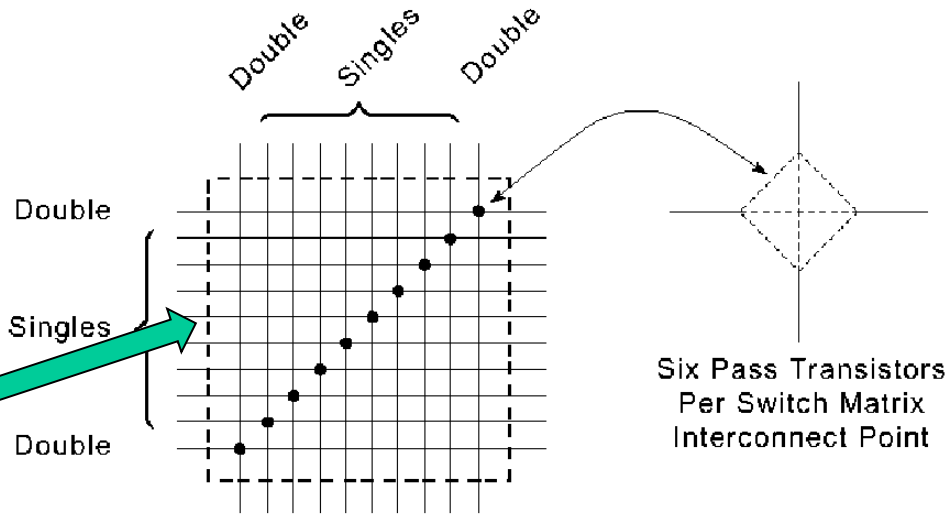
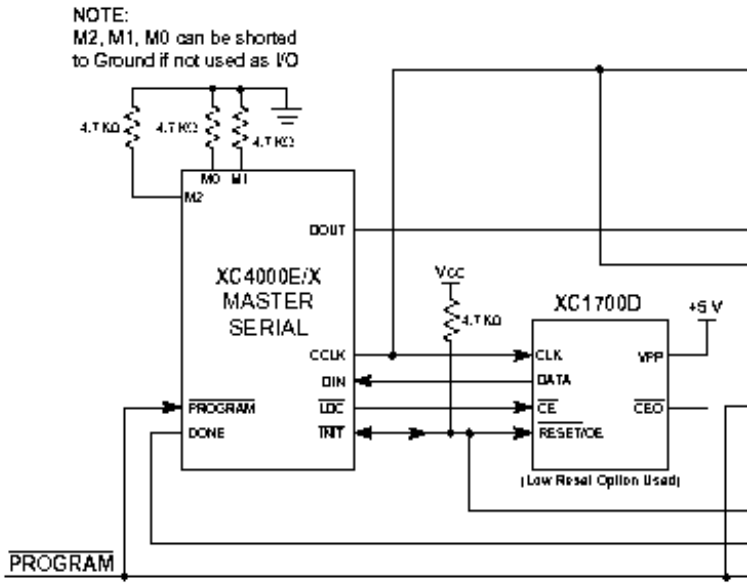


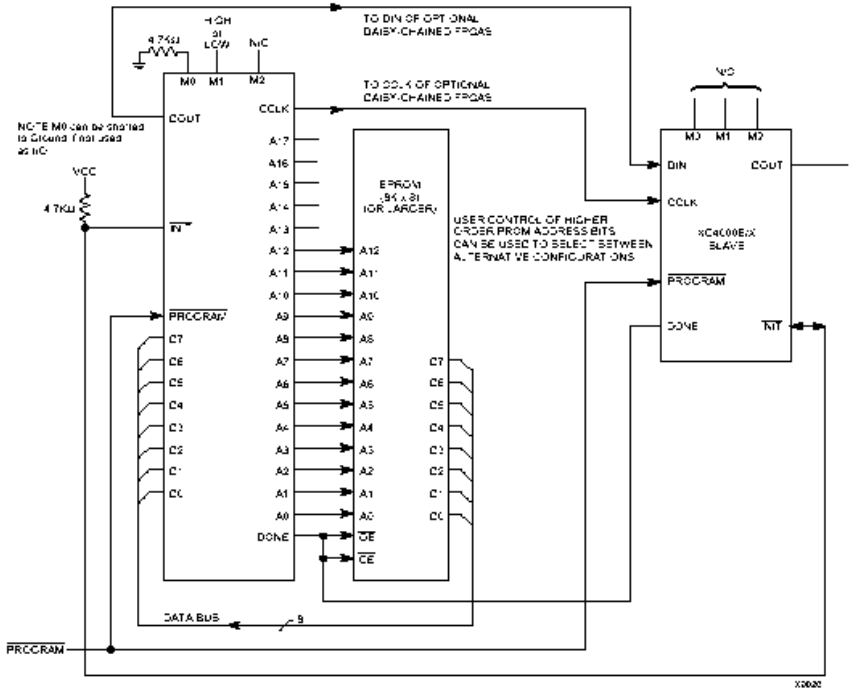
Figure 28: Single- and Double-Length Lines, with Programmable Switch Matrices (PSMs)

7) Circuits LSI: XILINX famille 4000

Configuration

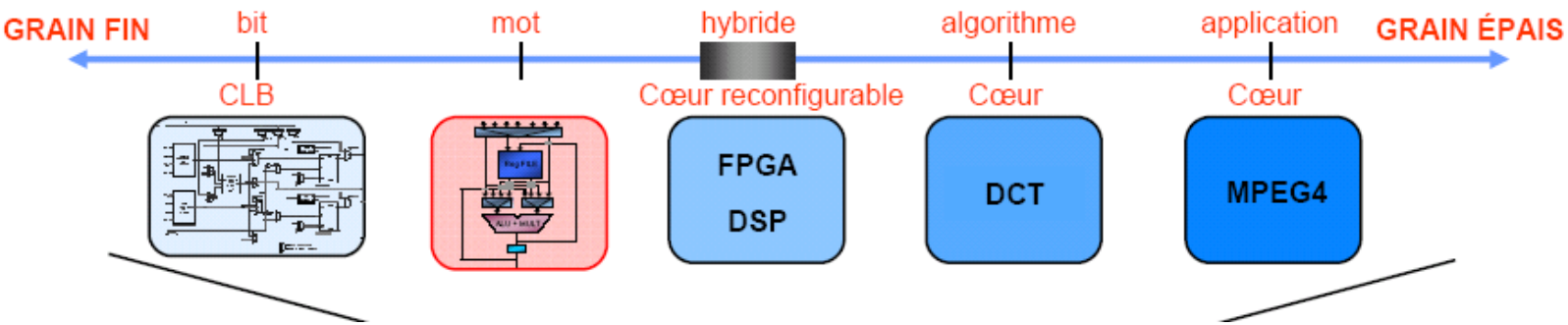


Master/Slave Serial Mode Circuit Diagram

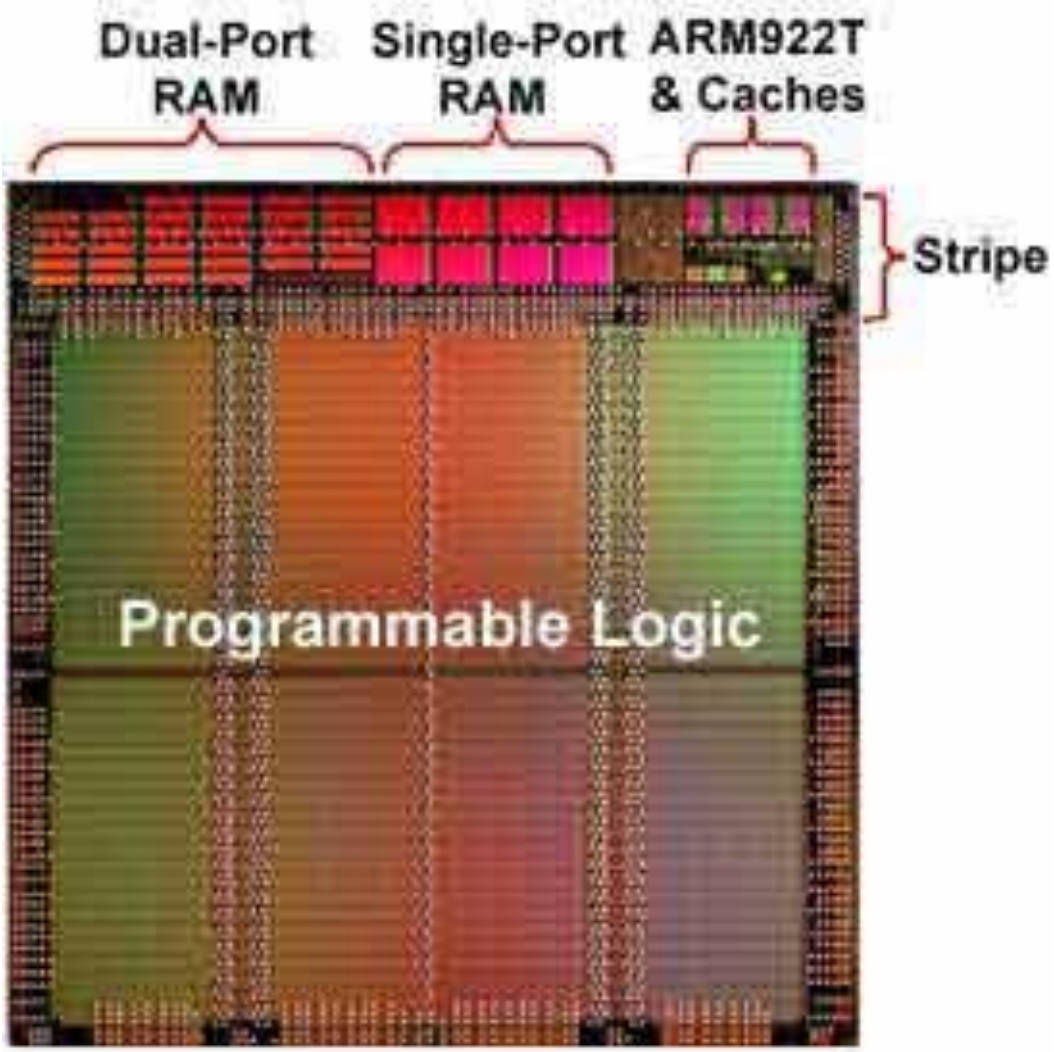


Master Parallel Mode Circuit Diagram

8) Du grain fin au grain épais

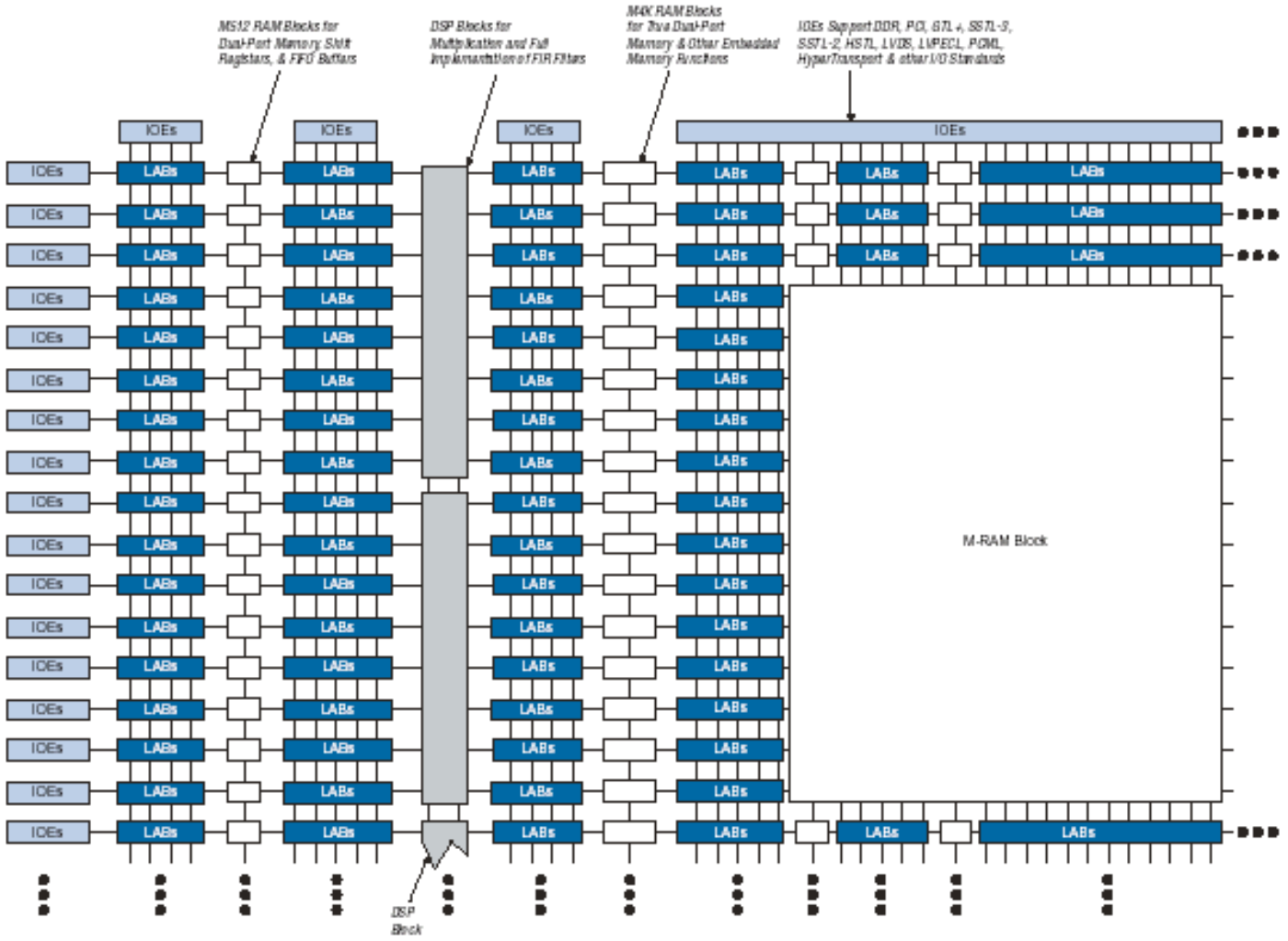


8) Circuits VLSI: ALTERA série Excalibur **Architecture ARM**



8) Circuits VLSI: ALTERA série Stratix Architecture DSP

Figure 1. Stratix Block Diagram



8) Circuits VLSI: ALTERA (séries Stratix, Cyclone, …)

Intégration de:

- PLL
- Cœurs de processeurs
- Multiplieurs accumulateurs
- Blocs IP (FFT, USB2, cœurs de processeurs sous forme IP, …)

Select a Nios II core:

	○ Nios II/e	◉ Nios II/s	○ Nios II/f
Nios II Selector Guide Family: Stratix f_{system}: 0,0 MHz cpuid: 0	**RISC** **32-bit**	RISC 32-bit **Instruction Cache** **Branch Prediction** **Hardware Multiply** **Hardware Divide**	RISC 32-bit Instruction Cache Branch Prediction Hardware Multiply Hardware Divide **Barrel Shifter** **Data Cache** **Dynamic Branch Prediction**
Performance at 0,0 MHz	Up to 0 DMIPS	Up to 0 DMIPS	Up to 0 DMIPS
Logic Usage	600-700 LEs	1200-1400 LEs	1400-1800 LEs
Memory Usage	Two M4Ks (or equiv.)	Two M4Ks + cache	Three M4Ks + cache

8) Circuits VLSI: ALTERA série Stratix

Configuration des sorties

Figure 70. Termination Schemes for Single-Ended I/O Pins

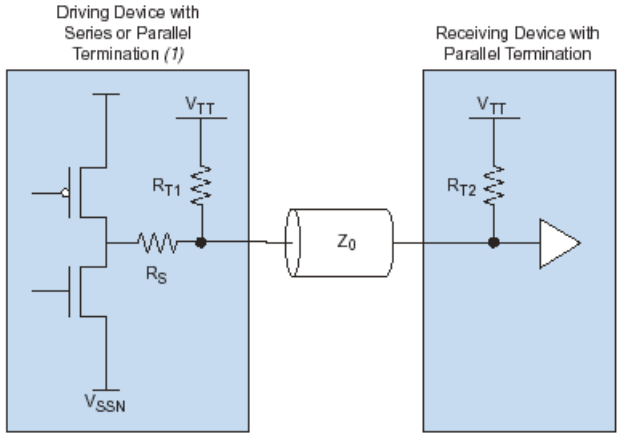
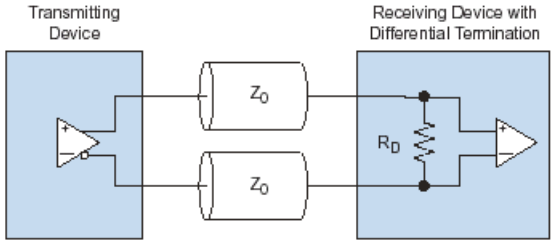


Figure 71. Differential LVDS Input On-Chip Termination



9) Evolution des tensions d ’alimentation et des technologies

A ce jour: plus de quatre millions de portes !!!

Tensions d ’alimentation: 5V pour les premières générations à 3.3V, 2.5V puis 1.8V , 1.5V et 1.2V (0.13µm). **Aujourd’hui: 40nm puis 28nm !!**

Les circuits de dernière génération (exemple: familles APEX, STRATIX d ’ALTERA) sont dits « MULTI-I/O » et peuvent être interconnectés avec des familles de technologies différentes.

LVTTL: Low Voltage TTL

LVCMOS: Low Voltage CMOS

GTL+: Gunning transceiver logic

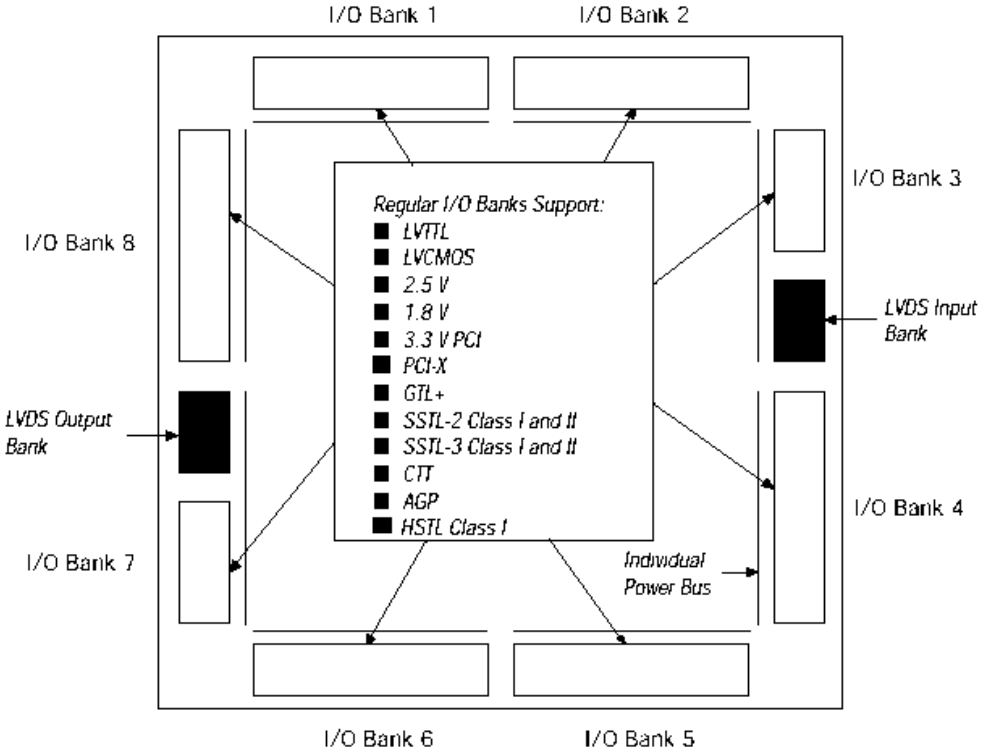
SSTL: Stub Series Terminated Logic

CTT: center Tap Terminated

AGP: Advanced Graphic Port

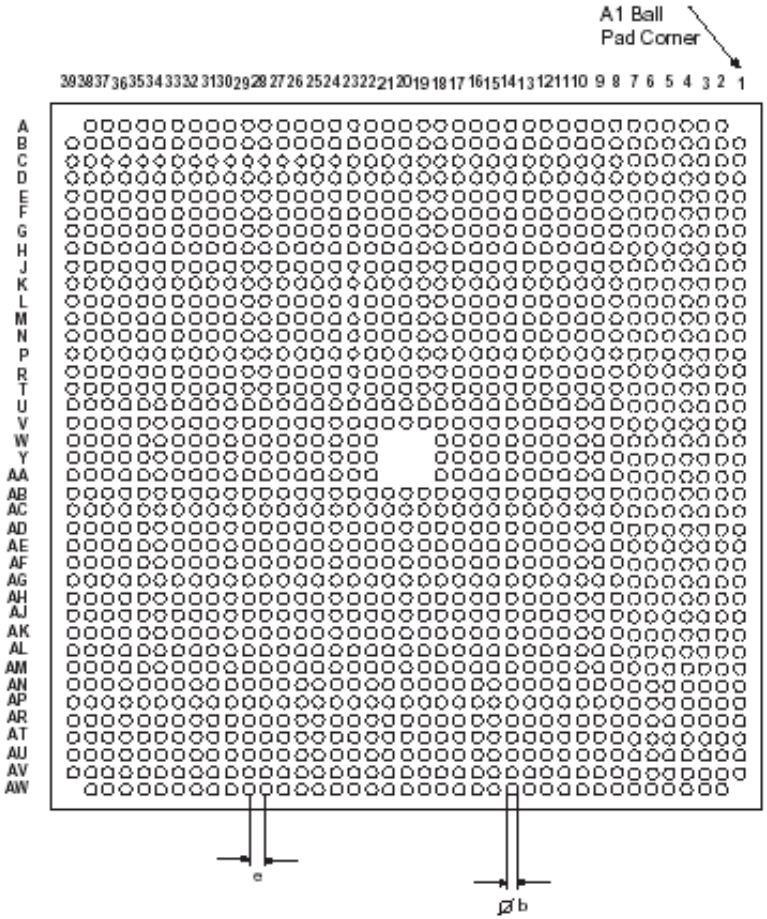
HSTL: high Speed Transceiver Logic

LVDS: low Voltage differential Signal

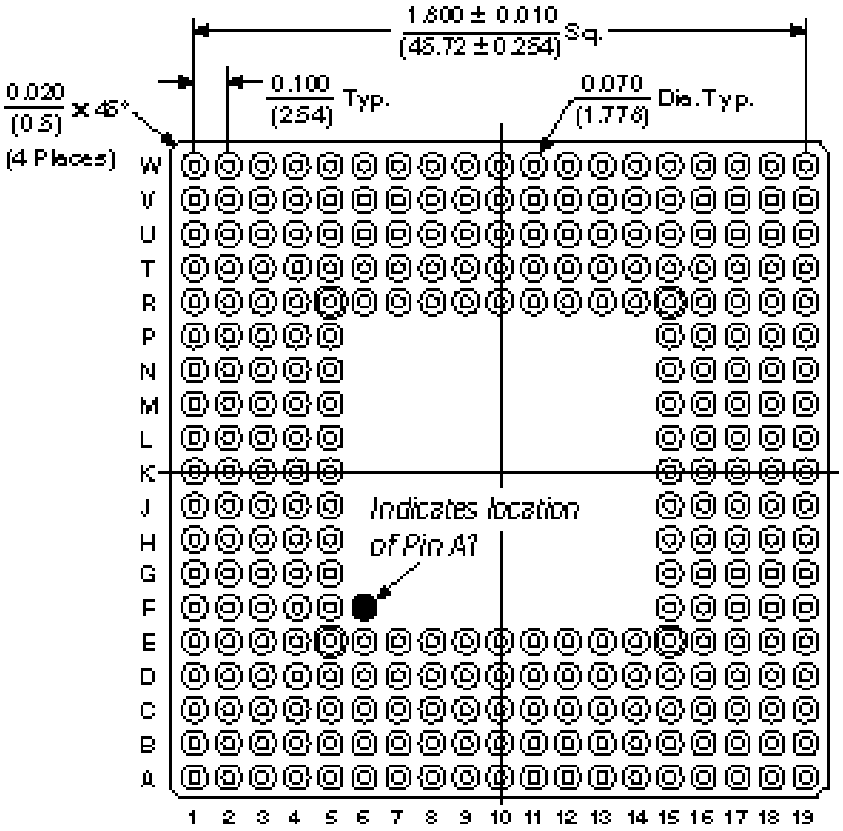


10) Boîtiers

BGA 1548 pins (40mm)

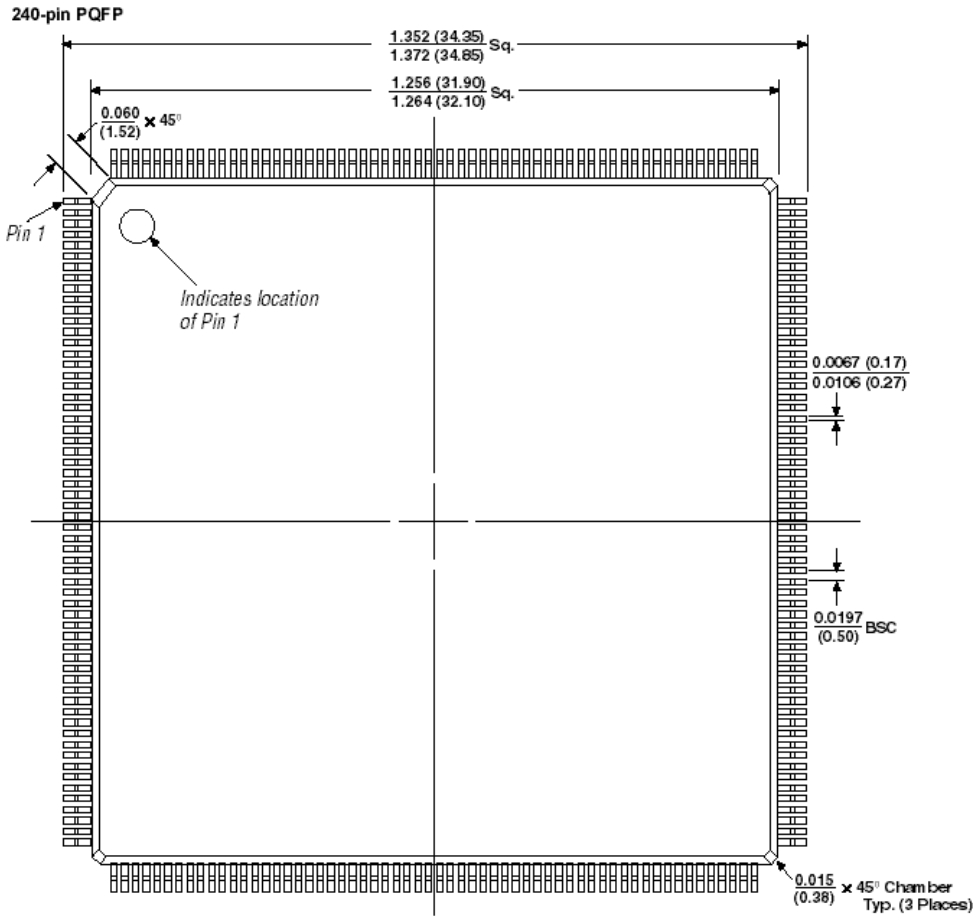


PGA 280 pins



10) Boîtiers:

240 PQFP



AVANTAGES DES CIRCUITS PROGRAMMABLES.

- **LA COMPACITE**
- **LA CONSOMMATION**
- **LES TEMPS DE PROPAGATION**
- **LA SIMPLIFICATION DE L ’ETUDE DU CI**
- **LA SIMPLIFICATION DE LA FABRICATION DU CI**
- **LA SIMPLIFICATION DU CÂBLAGE**
- **LA REDUCTION DES STOCKS**
- **LA REDUCTION DU TEMPS DE DEVELOPPEMENT (Time to Market)**
- **COÛT GRANDE SERIE (boîtiers OTP)**
- **LA CONFIDENTIALITE**
- **LA CEM**
- **L ’EVOLUTIVITE**
- **LA RECONFIGURABILITE**
- **LA TESTABILITE (interface JTAG)**

11) Les outils de synthèse.

- Equations logiques
- Tables de vérité
- Machines à état
- Schémas (symboles graphiques)
- Langages (VHDL, AHDL, VERILOG, SystemC, …)

VHDL: STANDARD reconnu par l 'IEEE
norme IEEE-1076 (1987)
et IEEE-1164 (1993)

12) Les tendances.

- Apparition de compilateurs C => VHDL voire SystemC => VHDL

⇒ TRITON (Poseidon Design Systems)

⇒ GAUT (LESTER Université de Bretagne Sud)

⇒ CATAPULT C (Mentor Graphics)

⇒ IMPULSE C (Impulse Accelerated Technologies)

⇒ PICO (Symphora)

⇒ UGH (Tima/Lip6)

⇒ DK design suite (Celoxica)

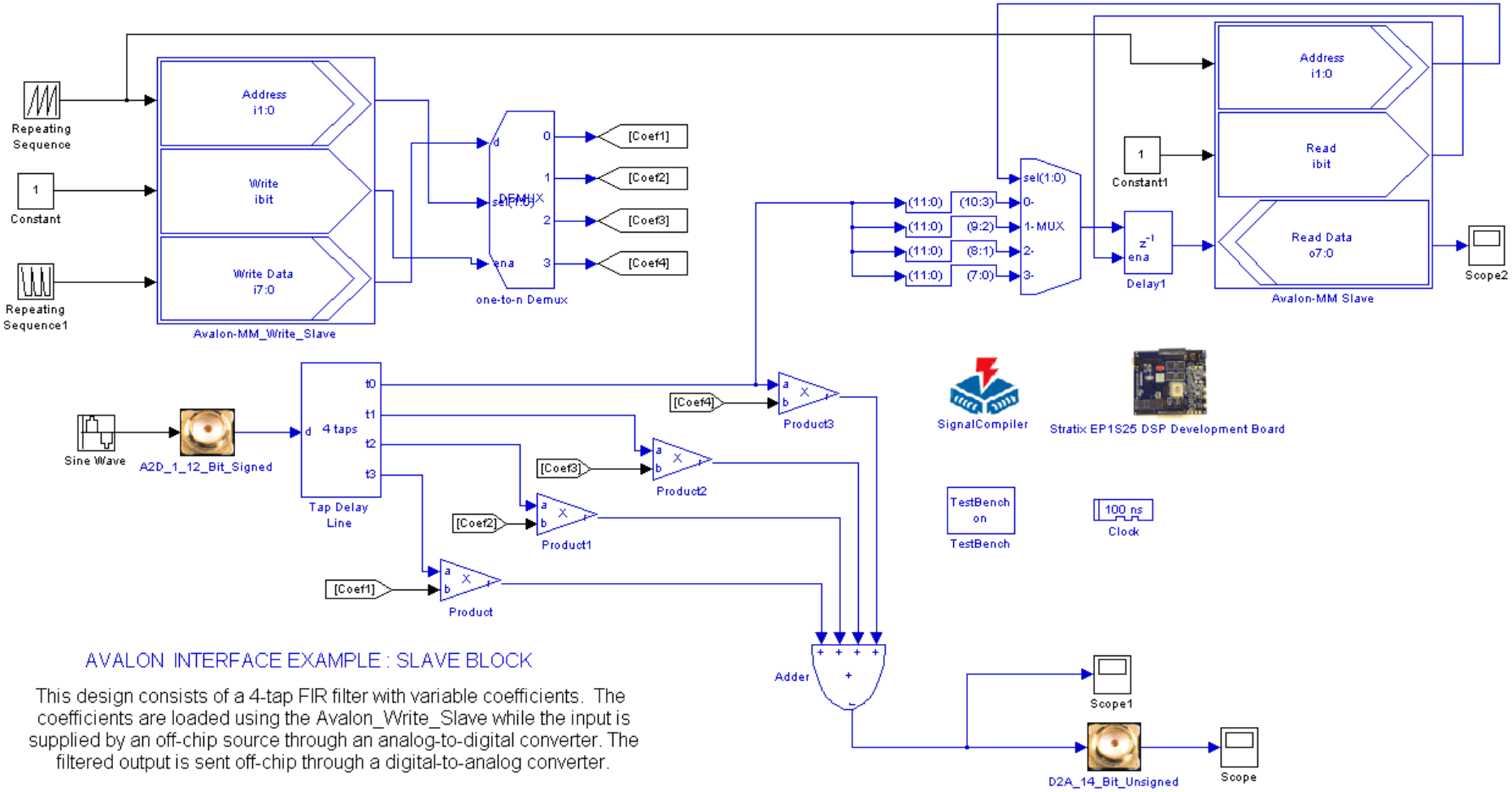
⇒ ...

12) Les tendances.

- Conception niveau Système:

- DSP Builder (Altera)
- Synplify DSP (Synplicity)
- XN Generator
- Simulink HDL

12) Les tendances. - Conception niveau Système:



AVALON INTERFACE EXAMPLE : SLAVE BLOCK

This design consists of a 4-tap FIR filter with variable coefficients. The coefficients are loaded using the Avalon_Write_Slave while the input is supplied by an off-chip source through an analog-to-digital converter. The filtered output is sent off-chip through a digital-to-analog converter.